memory controller bus 216 allows memory access requests, as well as data, to be passed between the two memory controllers 402 and 422. Each of the memory controllers 402 and 422 is coupled to an addressable memory area 412 and 432, respectively, that is defined by two values. The two values are stored in registers 404a-b and 406a-b. Registers 404a and 406a of the memory controller 402 store the start address and memory size for the addressable memory area 412, and registers 404b and 406b of the memory controller 422 store the start address and memory size value for the addressable memory area 432. These values are referenced by the respective memory controller to determine whether a memory access request is to a memory location in the addressable memory area to which the memory controller is coupled.--

REMARKS

The amendments to the specification are made to complete the reference to the aforementioned co-pending application.

Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached page is captioned **"Version with Markings to Show Changes Made"**.

Respectfully submitted,

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KNE:sem
Enclosures:
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Information Disclosure Statement
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the specification:

Paragraph beginning at line 1 of page 9 has been amended as follows:

Figure 4 illustrates a distributed memory controller memory subsystem 400 that may be substituted into a graphics processing system. A more detailed description of a similar memory subsystem is provided in Patent Application [No. _____, filed _____, which] No. 09/603,158, filed June 23, 2000, which is incorporated herein by reference. To summarize, the memory subsystem 400 includes two memory controllers 402 and 422 coupled together through a memory controller bus 216. The memory controller bus 216 allows memory access requests, as well as data, to be passed between the two memory controllers 402 and 422. Each of the memory controllers 402 and 422 is coupled to an addressable memory area 412 and 432, respectively, that is defined by two values. The two values are stored in registers 404a-b and 406a-b. Registers 404a and 406a of the memory controller 402 store the start address and memory size for the addressable memory area 412, and registers 404b and 406b of the memory controller 422 store the start address and memory size value for the addressable memory area 432. These values are referenced by the respective memory controller to determine whether a memory access request is to a memory location in the addressable memory area to which the memory controller is coupled.